REMARKS

Claims 1-17 are pending. Applicant has amended claims 1, 7, and 13-17 and added claims 18-20 herein.

The Examiner indicated that copies of some references on the Information Disclosure Statement (IDS) filed January 12, 2004 were not provided. However, applicant notes that each reference included in the IDS is listed on pp 1-3 of the parent patent. Accordingly, applicant respectfully requests that this objection be withdrawn.

The Examiner indicated that several elements of the specification and figures were not in compliance. Applicant has amended the specification and figures herein to comply with the changes requested by the Examiner. Accordingly, applicant respectfully requests that this objection be withdrawn.

The Examiner rejected claims 1-3, 5-9, and 11-12 are rejected under 35 U.S.C. § 103(a) over Borkenhagen et al. (U.S. Patent No. 6,567,839) in view of Sharangpani et al. (U.S. Patent No. 6,272,520) and claims 4, 10, and 13-17 over Borkenhagen, Sharangpani, and Hogle et al. (U.S. Patent No. 6,560,626). Applicant respectfully traverses this rejection.

Borkenhagen describes a technique for reducing memory latency due to cache misses in multithreaded processor systems. The system in Borkenhagen is a typical multi-threaded processor system in which multiple threads share processor resources. An operating system provides time slices to each thread and swaps the threads in and out based on various algorithms. Borkenhagen does not describe a system in which the operating system coordinates swapping in and out with the thread. Sharangpani describes a method for detecting thread switch events based on whether a cache miss has occurred, and also does not describe a system in which the operating system coordinates with the thread to swap the thread in and out.

In contrast, applicant's technology describes a processor architecture that defines multiple simultaneously executing protection domains. Each protection domain defines the program memory, data memory, and number of streams that are allocated to computations that use the processor. Specification, paragraph [0007]. When executing tasks within this architecture, special techniques are required to swap tasks in and out of a protection domain. These techniques are the subject of applicant's claims. In some embodiments, the task itself is used to ensure that the task is ready to be swapped out (e.g., by ensuring a proper state of the memory it is using). In such embodiments, the task is notified of low-level task switching decisions that are not typical in other systems.

Claim 1 recites "notifying a task executing on a parallel processor architecture having multiple simultaneously executing protection domains that the task is being preempted from utilizing the processor." In most multithreaded processor systems, the operating system simply preempts a thread whenever it chooses, and swaps in another thread. The operating system then handles the preservation of the thread's state. However, because of the nature of the protection domains defined by applicant's technology, it is desirable to coordinate with the task to swap the task out so that the task can preserve various elements of its executing state within the protection domain, "[t]he swapping in and swapping out of tasks requires cooperation on the part of the task." Specification, paragraph [0053]. Borkenhagen does not describe a task executing within a protection domain, or notifying the task that it is being preempted. Rather, in the sections relied upon by the Examiner, Borkenhagen describes swapping out a task using a "thread switch manager" that is external to the task and that does not notify the task that the task is being preempted. Likewise, Sharangpani uses a "thread switch module" external to the threads to determine when and how to swap threads. Sharangpani does not describe notifying a task that the task is being preempted. Therefore, applicant's claims are patentable over the combination of Borkenhagen and Sharangpani. Accordingly, applicant respectfully requests that these rejections be withdrawn.

Based upon these remarks and amendments, applicant respectfully requests reconsideration of this application and its early allowance. If the Examiner has any questions or believes a telephone conference would expedite prosecution of this application, the Examiner is encouraged to call the undersigned at (206) 359-3265. Applicant believes all required fees are being paid in connection with this response. However, if an additional fee is due, please charge our Deposit Account No. 50-0665, under Order No. 324758001US2 from which the undersigned is authorized to draw.

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Respectfully submitted,

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